REDUCING JITTER IN MIXED-SIGNAL INTEGRATED CIRCUIT DEVICES

[ABSTRACT OF THE DISCLOSURE]

A data converter is implemented as an integrated circuit device (100). The converter comprises signal processing circuitry (120-170) which produces an output signal (OUT) in dependence upon a received input signal (D1-Dm). Production of the output signal (OUT) is initiated at a time determined by a timing signal (CLK) and is completed at a time which is delayed by a delay time with respect to the timing signal (CLK). A delay-contributing portion (130, 150, 160) makes a contribution to the delay time that is affected by variations in a power supply voltage (VDD) applied thereto. An internal supply voltage regulator (110) derives a regulated internal power supply voltage (VDD(REG)) from an external power source voltage (VDD), and applies this voltage to the delay-contributing portion (130, 150, 160) to fix its contribution to the delay time at some value independent of variations in the external power source voltage. At least one further circuitry portion (140, 170) within the integrated circuit device (100) is powered by a supply voltage (VDD) other than the regulated internal power supply voltage (VDD(REG)).